A 2.4GHz SINGLE CHIP TRANSCEIVER

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Abstract

A single chip, GaAs transceiver is described. The circuit includes all transmit and receive switching, amplification, frequency conversion and level shifting. An on chip oscillator is also provided. Low receive current of 30mA from a +5V supply and a standby current of less than 0.5mA, make this an ideal component for battery powered operation.

Introduction

The Industrial, Scientific and Medical (ISM) frequency band includes the frequency range 2.4 - 2.483GHz. In the USA, unlicensed operation using spread spectrum modulation at transmitter powers of up to 1W is permitted over this band. This paper describes a transmit/receive front end for a 2.4GHz wireless communications transceiver, the entire circuit of which has been integrated onto a single GaAs MMIC. A photograph of the 3.3mm x 5.2mm chip, which is available in an SSOP-28 style plastic package, is shown in Figure 1.

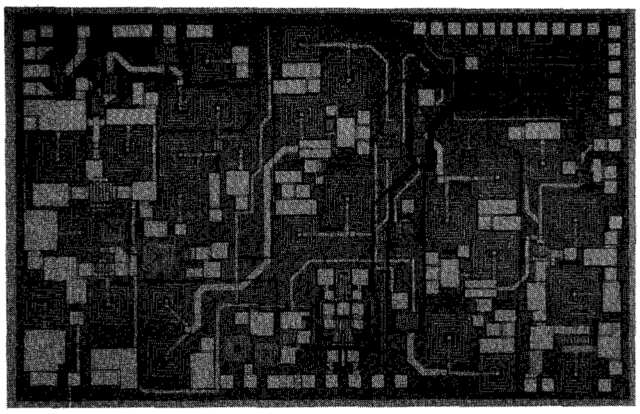

Figure 1 Photograph Of The Transceiver MMIC

Transceiver Architecture

A block diagram of the complete transceiver is shown in Figure 2. The circuit can be switched between receive, transmit and standby states. In receive mode, RF input signals are downconverted to differential IF signals. Although designed specifically for the 2.4-2.5GHz band, RF signals between 1.9GHz and 2.6GHz can be accommodated. The off chip filters can be selected to suit the band of interest.

In transmit mode, the IF input signal can be between 100MHz and 600MHz. The balanced input is upconverted to a single ended signal at the RF frequency. The circuit has been designed to provide a constant output power for a wide range of IF signal levels. A switched attenuator has been included to allow a 10dB step in the output power level.

The frequency of the VCO, and hence the IF frequency, is selected by appropriate choice of an off-chip resonator. Local oscillator frequencies of between 1.4GHz and 2.7GHz are available. A diversity switch has also been included to allow antenna selection. DC supply to the chip is +5V and -5V, with

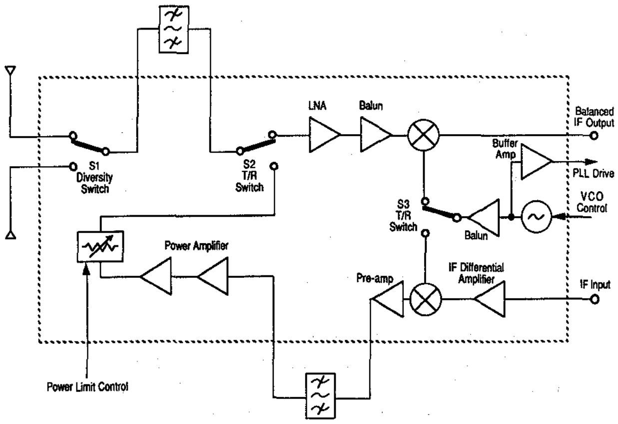

Figure 2 Block Diagram Of The Transceiver

complementary 0V/-5V switching. The -5V supply takes less than 1mA of current, regardless of transceiver operating mode. Typical current requirements from the +5V supply are 30mA in receive mode and 220mA in transmit mode. A standby state is also available and requires a current of less than 0.5mA.

In addition to the complete transceiver chip, all of the sub-circuits have been manufactured as individually measurable components. The design and measured performance of these subcircuits is described below. The circuits were realised on the standard GMMT F20 depletion mode GaAs MMIC process.

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Sub-Circuit Design and Measurements

LNA: The Low Noise Amplifier (LNA) is a two stage design with series inductive feedback to allow good noise figure performance with a well matched input[1]. A stacked bias arrangement is used to help reduce current consumption. Instead of biasing the drain of each FET at +5V and the source at 0V, the arrangement shown in Figure 3 is used. This allows the +5V to be shared between the FETs and the current to be re-used. The RF On Wafer (RFOW) measured s-parameters of a

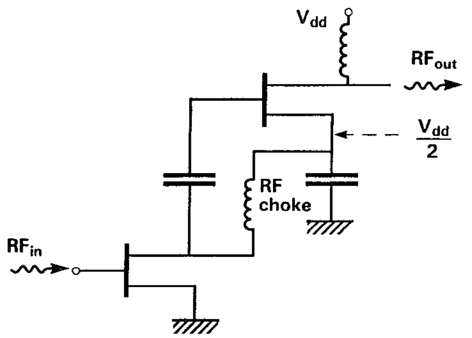

Figure 3 **Stacked Bias Arrangement**

typical LNA are shown in Figure 4. Gain is 17.5dB ±0.5dB from 2 - 3GHz. The input match is better than 15dB and the output match is better than 13dB. Measured noise figure is 2.5dB at 2.4GHz. Total current consumption is 6mA from a +5V supply.

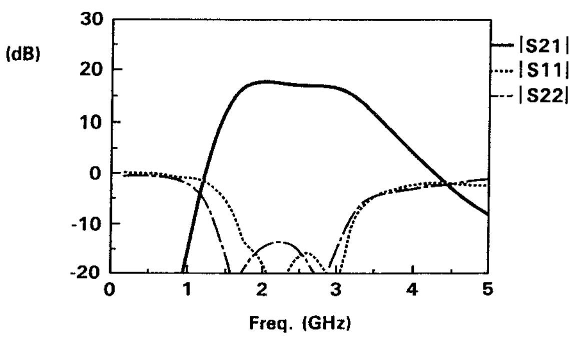

Figure 4 **RFOW Measured s-parameters of LNA**

Switches: T/R and diversity switches all use simple series mounted FETs[2]. The drain and source of each FET is biased at zero volts DC and the control signal is applied to the gates. One common design of Single Pole Double Throw (SPDT) switch is used throughout. The measured "on" case insertion loss at 2.4GHz is typically 0.7dB with an "off" case isolation of 20dB.

Mixers: A quad ring of zero biased FETs is used to realise a balanced conductance mixer[3]. When driven with differential inputs, excellent balance is achieved with a conversion loss of 6dB.

VCO: A Clapp type Voltage Controlled Oscillator (VCO) is used[4]. The oscillation frequency can be set between 1.4GHz and 2.7GHz by an external resonator. An off chip varactor allows an instantaneous voltage controllable tuning range of 150MHz. For RFOW testing of the subcircuit an inductor/capacitor combination was included on-chip, for use as an alternative to the off-chip resonator.

Active Baluns: Active baluns are used for both the RF and LO signals. Each balun uses a common gate stage and a common source stage of amplification to provide an equal amplitude split with 180° phase difference[5]. Figure 5 shows the RFOW measured s-parameters of a typical LO balun and Figure 6 shows the insertion phase between the input and each of the two outputs. A gain of 1dB at 2.1GHz and terminal matches of better than 20dB is achieved. The amplitude difference is only

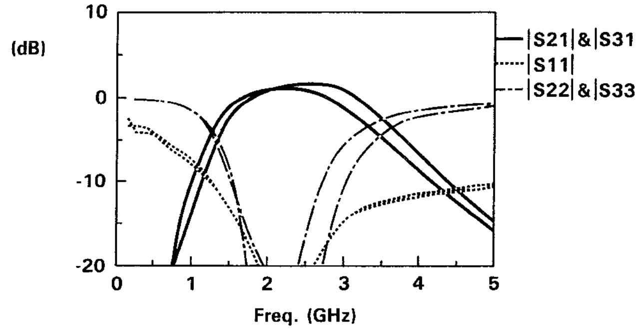

Figure 5 **RFOW Measured s-parameters of LO Balun**

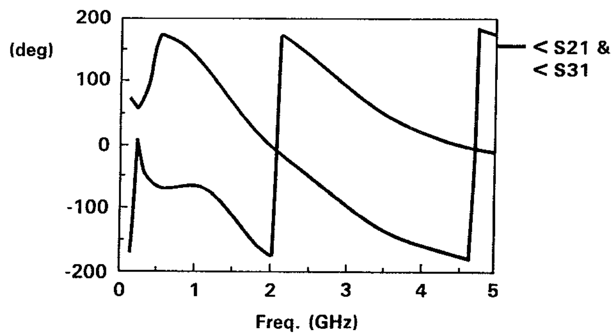

Figure 6 **RFOW Measured s-parameters of LO Balun**

0.15dB and the phase difference is 186°. Stacked bias has been used to allow operation with only 6mA of current from a +5V supply. The RF balun is of the same design but with a centre frequency of 2.4GHz.

Buffer Amplifier: The buffer amplifier is used to provide a low level output for phase locking of the LO. It must present minimal loading to the VCO, provide high isolation and be able to operate into any load from 50Ω to an open circuit. This has been achieved by using a small, single finger FET, biased through a 50Ω resistor in the drain. The reverse isolation is more than 40dB at 2.4GHz and the output match is better than 14dB. An insertion loss through the buffer of 12.5dB ensures the required low level of output power is delivered. Current consumption of this component is only 1.5mA.

Differential Amplifier: With the chip in transmit mode, the IF input is into a two stage differential amplifier[6,7]. Active biasing is used throughout in order to minimise chip area. The differential input impedance to the circuit is 800Ω. When driven with differential signals from a source of the same impedance, the gain of the amplifier is 20dB over a frequency range of 100MHz to 500MHz.

Pre-amplifier: The output of the transmit mixer is amplified by the pre-amplifier prior to passing off chip, through the transmit filter and into the power amplifier. A low level of gain is required to balance the gain budget through the transmit chain. The input to the pre-amp is resistivity matched with reactive matching at the output. The amplifier exhibits a flat 5dB of gain from 2 - 3GHz. Input return loss is greater than 12dB and output return loss is greater than 17dB.

Power Amplifier: A two stage power amplifier is used to increase the level of the transmit signal[4]. Figure 7 shows the small signal s-parameters of the amplifier. The gain is 23dB at 2.4GHz with input and output return losses of greater than 13dB.

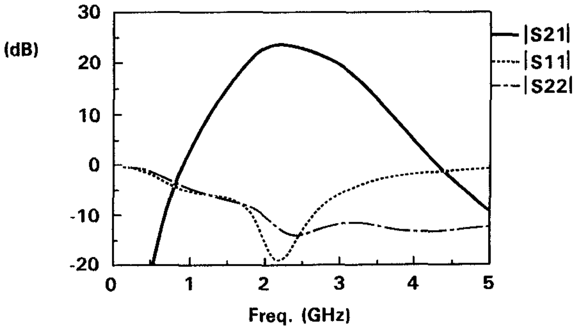

Figure 7 RFOW Measured s-parameters of Power Amplifier

Switched Attenuator: A 10dB switched resistive attenuator[8] is positioned before the common T/R port in the transmit path. This allows the output power level to be switched by 10dB. The small signal gain through the power amplifier, attenuator and T/R switch on the complete transceiver chip has been measured with the attenuator in both states. Figure 8 is a plot of this and the 10dB gain difference shows the accuracy of the switched attenuator. Because the attenuator is positioned after the power amplifier it gives an accurate 10dB step in output power level, regardless of amplifier compression.

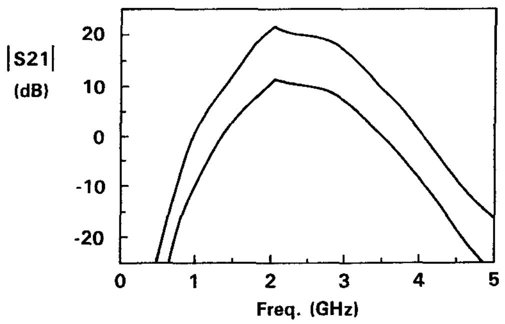

Figure 8 Measured Gain Of Power Amp, Attenuator and T/R Switch Chain, Two States

Transceiver Measurements

Measurements have been made on the complete transceiver chip. These were made on an unpackaged device in a purpose built jig. A spectral plot of the buffer amplifier output is shown in Figure 9. The output power level is -12dBm with a phase noise

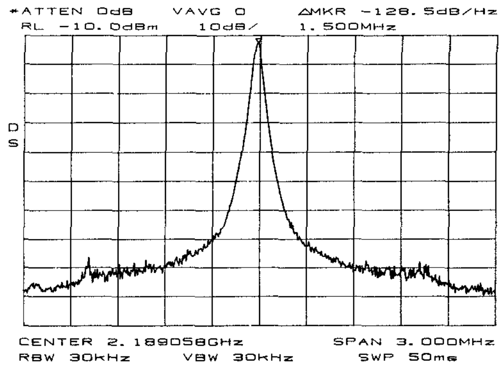

Figure 9 LO signal at Buffer Amplifier Output

of -122dBc/Hz at 1MHz off carrier. This signal is used to drive the phased lock loop of the transmit/receive circuit.

Figure 10 shows the measured receiver conversion gain and double sideband noise Figure versus IF frequency. This is for a fixed LO frequency of 2.035GHz with the IF varying from 50MHz to 500MHz. The slight roll off with increasing IF frequency is a result of losses in the chip and jig IF paths and in the balun used to combine the differential IF signals.

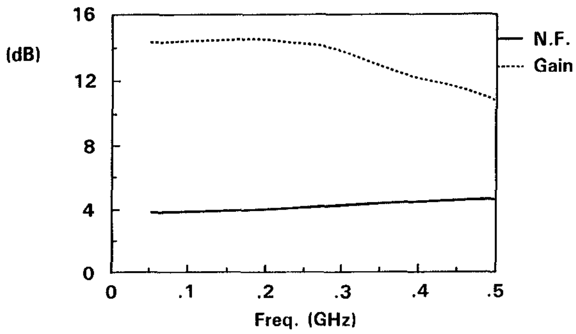

Figure 10 Measured Receiver Gain and DSB Noise Figure

The power transfer characteristic through the power amplifier, attenuator and T/R switch chain has been measured and is shown in Figure 11. A saturated output power capability of +21dBm is demonstrated. In practice the chip is designed to operate in saturation with a constant output power level. This reduces chip to chip variation, improves efficiency and allows a

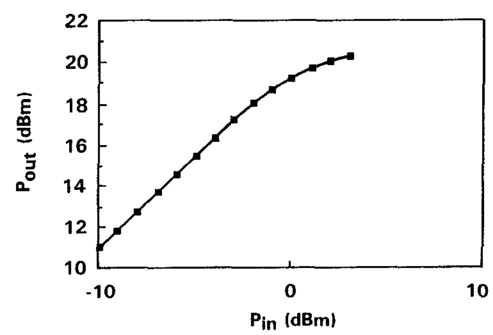

Figure 11 Power Transfer Characteristic Of Power Amp Attenuator and T/R Switch Chain

large tolerance to the range of IF input signals. Figure 12 shows the small signal gain versus IF frequency through the entire transmit chain from differential IF input to T/R common port output. This was measured with the LO frequency fixed at 2.035GHz and shows a gain of 38dB ±1dB for IF frequencies between 100MHz and 500MHz.

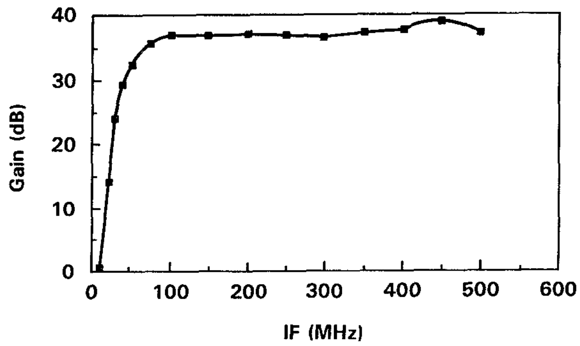

Figure 12 **Small Signal Gain Of Transmit Chain Versus IF Frequency**

Future Enhancements

Several enhancements to the circuit architecture have now been implemented and the modified design is currently being manufactured. In particular the input referred third order intercept point (IP3) has been increased from the present -10dBm to -3dBm. This was achieved by replacing the active baluns with passive networks, increasing the gain and linearity of the LNA, including on-chip diplexer filters to terminate properly the mixer IF ports and introducing a receive chain IF amplifier to balance the gain budget and match the output to a higher impedance. A further consequence of using passive baluns is that a single mixer is now used for both transmit and receive modes of operation. A block diagram of the modified transceiver architecture is shown in Figure 13.

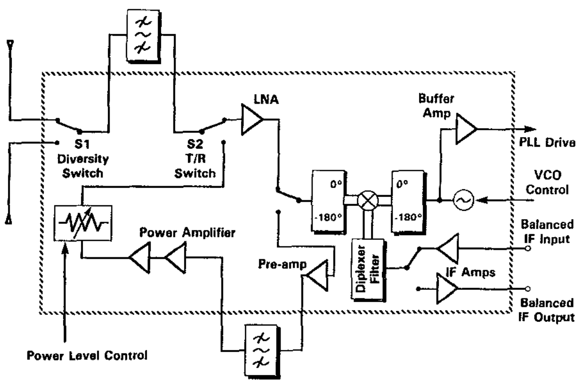

Figure 13 **Enhanced Transceiver Architecture**

Conclusions

A single chip GaAs transceiver to cover the 2.4 - 2.483GHz ISM band has been described. Receive gain is 13dB with differential IF outputs and a double sideband noise figure of 4dB. Current consumption in receive mode is just 30mA from a +5V supply. A standby mode is available with a current consumption of less than 0.5mA. Transmit mode offers a constant output power level, switchable by 10dB, for a large range of IF input levels. These features combine to give a component which is ideally suited to spread spectrum Wireless LAN applications. The chip is available in a low cost SSOP-28 style plastic package (Figure 14).

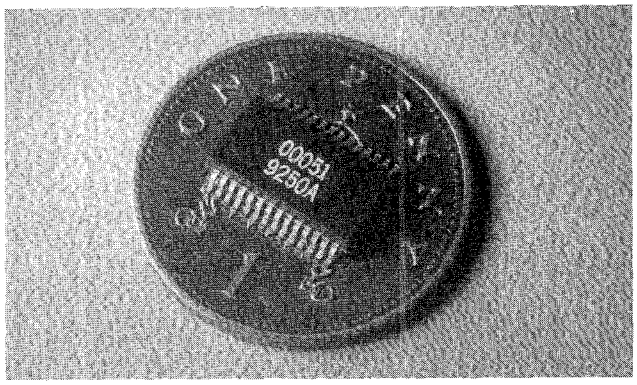

Figure 14 **Transceiver MMIC in SSOP-28 Plastic Package**

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